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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,853	TAGO ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *17 June 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE and Amendment as received on 7/9/2004.

Non-Compliance

3. Applicant's amendment filed on July 9, 2004, fails to comply with revised 37 CFR 1.121. More specifically, applicant appears to be replacing portions of the claims without indicating deletion of the replaced material. For instance, in claim 1, line 11, applicant replaces "sequence" with "sequences" without indicating deletion of "sequence" (via strikethrough or double brackets). Likewise in line 14, "the" is replaced with "a" without deleting "the". Finally, some of the numbers of claim 1 (29, 15, C1, etc.) were indicated as added by underlining. Please see http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/officeflyer.pdf for further details.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The examiner recommends incorporating the idea of the multiple buffers and their purposes into the title.

Drawings

5. The drawings field on July 9, 2004 are objected to because it is not clear as to how or what applicant is amending. There are some scribble marks on the circles, but the examiner does not understand what this represents. Please submit formal drawings including applicant's desired amendments.

Claim Comments

6. The examiner has again reviewed applicant's claims to the best of his ability and has found many grammatical errors and 112 problems (antecedent basis, indefiniteness), some of which were presented to and overlooked by applicant in the previous Office Action. The examiner does not have the time or resources to identify every mistake made on applicant's behalf but has so far done so in order to help applicant achieve clear claims, and ultimately a quality patent. The examiner strongly urges applicant to review the claims before submitting a response, because in the future, the examiner may simply give an "idiomatic English" objection.

Claim Objections

7. Claim 1 is objected to because of the following informalities:

Please indent line 4 for clarity.

In line 8, applicant refers to reference number 29 when describing the instruction execution unit. However, the examiner cannot find number 29 in the figures. Does applicant mean to replace "29" with --20--?

In line 26, replace "following to the" with --following the--.

In the last paragraph, a word needs to be inserted before "either".

8. Claim 2 is objected to because of the following informalities:

Replace the first occurrence of "(04)" with --(02)--.

The 3rd to last paragraph is not clear as applicant repeats the phrase "instruction sequence (C1) is stored in either one of the". The examiner assumes that applicant will delete one occurrence of the repetitive phrase.

Insert a comma or semicolon at the end of the 2nd to last paragraph.

In the 2nd to last line, replace "execution result" with --an execution result--.

In the 2nd to last line, the examiner believes "(04)" should be replace with --(02)--.

9. Claim 3 is objected to because of the following informalities:

In line 2, replace "process" with --processed--.

In line 4, insert --(02)-- before "inside".

In the 3rd to last line of the 1st paragraph, the examiner believes "(12)" should be replaced with --(21)--.

In the 2nd to last line of the 1st paragraph, insert --(12)-- before "inside".

In the 2nd line of the 3rd paragraph, insert --said-- before "first".

In the 2nd to last line of the 3rd paragraph, replace "have" with --has--.

In the last line of the 3rd paragraph, replace "buffer" with --buffers--.

In the last paragraph, replace "buffer" with --buffers--.

10. Claim 4 is objected to because of the following informalities:

In line 5, replace "buffer" with --buffers--.

In paragraph 3, replace both occurrences of "buffer" with --buffers-- and replace "have" with --has--.

In the last paragraph, replace "buffer" with --buffers--.

11. Claim 6 is objected to because of the following informalities:

In line 11, replace "sequence" with --sequences--.

In line 15, remove "the".

In the 3rd to last paragraph, replace "following to the" with --following the--.

Finally, in the 4th to last paragraph, line 4, replace "(C2)" with --(02)--.

12. Claim 7 is objected to because of the following informalities: In line 2, replace "aid" with --said--.

13. Claim 8 is objected to because of the following informalities: Please replace "a branching prediction" with --the branching prediction--.

14. Claim 9 is objected to because of the following informalities: In the 2nd to last line, replace "sequenced" with --sequence--.

15. Claim 16 is objected to because of the following informalities: In line 1, the phrase "with a pipeline processing" is not understood.

16. Claim 14 is objected to because of the following informalities: In line 3, replace "an" with --and--.

17. Claim 15 is objected to because of the following informalities: In the last line, replace "eh" with an appropriate word.

18. Claim 16 is objected to because of the following informalities:

In line 1, the phrase "with a pipeline processing" is not understood.

In line 4, replace both occurrences of "sequences" with --sequence--.

19. Claim 18 is objected to because of the following informalities: In line 3, replace "of" with --or--.

Withdrawn Rejections

20. In response to applicant's amendment filed on July 9, 2004, the prior art rejections set forth in the previous Office Action are hereby withdrawn by the examiner. Applicant's arguments, while fully considered, are now moot. And, upon further consideration, a new grounds of rejection is applied below.

Claim Rejections - 35 USC § 112

21. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

22. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

23. Claim 1 recites the limitation "said instruction buffer" in the last paragraph. There is insufficient antecedent basis for this limitation in the claim because it is not clear which buffer applicant is referring to. Applicant should reword this portion of the claim such that it is clear that "said instruction buffer" is the buffer that has been invalidated.

24. Claim 2 recites the limitation "the first or second instruction buffers" in lines 17-18. There is insufficient antecedent basis for this limitation in the claim because first and second buffers were not previously disclosed (only a plurality of buffers was disclosed).

Claim 2 also recites the limitation "the branch target" in line 20. There is insufficient antecedent basis for this limitation in the claim.

Claim 2 recites the limitation "the first or second branch target address information buffers" in the 3rd to last paragraph. There is insufficient antecedent basis for this limitation in the claim because first and second information buffers were not previously disclosed (only a plurality of information buffers was disclosed).

Claim 2 recites the limitation "the branching instruction (12)" in the 2nd to last paragraph. There is insufficient antecedent basis for this limitation in the claim.

25. Claim 4 is unclear because it is not understood how a branching instruction inside the first sequence has multiple branch targets (lines 4-5). Claim 4 is further unclear because the examiner does not understand how a buffer and information is stored in the buffer (last 3 lines of the first paragraph).

Claim 4 recites the limitation "the branching instruction inside said first instruction sequence" in multiple places. There is insufficient antecedent basis for this limitation in the claim as instructions 02 and 04 have both been previously mentioned.

Claim 4 recites the limitation "the branching instruction inside said second instruction sequence" in multiple places. There is insufficient antecedent basis for this limitation in the claim as instructions 12 and 14 have both been previously mentioned.

Claim 4 recites the limitation "the fourth instruction sequence" in the 3rd paragraph. There is insufficient antecedent basis for this limitation in the claim.

26. Claim 6 recites the limitation "said instruction buffer" in the last paragraph. There is insufficient antecedent basis for this limitation in the claim because it is not clear which buffer applicant is referring to. Applicant should reword this portion of the claim such that it is clear that "said instruction buffer" is the buffer that has been invalidated.

27. Claim 8 recites the limitations "said branching instruction" and "the branching instruction." There is insufficient antecedent basis for this limitation in the claim because in claim 6, the applicant refers to both a first and second branching instruction.

28. Claim 9 recites the limitations "said branching instruction". There is insufficient antecedent basis for this limitation in the claim because in claim 6, the applicant refers to both a first and second branching instruction. Furthermore, is "a branching instruction" the same as "said branching instruction? If so, the claim should be modified to be more clear.

Claim Rejections - 35 USC § 102

29. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

30. Claims 1-4, 6-9, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Asato, U.S. patent No. 6,289,442.

31. Referring to claim 1, Asato has taught an information processing device which reads, buffers, decodes, and executes instructions from an instruction store portion by pipeline processing, comprising:

a) an instruction reading request portion which assigns a read address to said instruction store portion. See Fig.1, component 12, and column 5, lines 12-14.

b) an instruction buffering portion including a plurality of instruction buffers which buffer instruction sequences read from said instruction store portion. See Fig.1, components 22A-H (reservation stations). Reservation stations buffer instructions sequences and operands. Also, note instruction cache 16. A cache is essentially a large buffer with many entries. This can also be viewed as a number of sub-buffers.

c) an instruction execution unit which decodes and executes instructions buffered by said instruction buffering portion. See Fig.1 components 20 and 24A-H.

d) a branching instruction detection portion which detects a branching instruction inside the instruction sequences read from said instruction store portion. See lines 5-7 of the abstract and note that branches are detected by a "detection portion".

e) a branch target address information buffering portion including at least first and second branch target address information buffers which, when said branching instruction detection portion has detected a branching instruction, buffer a branch target address information for generating the branch target address of said branching instruction. See Fig.1, components 22A-H, Fig.6B, and column 11, lines 13-15. Note that target information is also stored in reservation stations. It should be noted from Fig.1 that there are a plurality of reservation stations (buffers), which are table-like memories. Clearly, each individual instruction will have its own separate buffer

location (entry in the table) within the reservation station. Hence, the branch target information buffers would comprise the reservation station entries dedicated to buffering the target path information.

f) wherein when said branching instruction detection portion detects a first branching instruction in a first sequence being processed, which is stored in one of said plurality of instruction buffers, a branch target instruction sequence of said first branching instruction is stored in another one of said plurality of instruction buffers and said first and second instruction sequences are fetched from said instruction store portion and stored in said plurality of instruction buffers. See Fig.6B, and note that when a first branch instruction A3 in the first sequence of instructions ("A" instructions) is encountered, a target sequence ("B" instructions) are fetched, tagged, and buffered.

g) when said branching instruction detection portion detects a next branching instruction following the first branching instruction in said first instruction sequence, a first branch target address information of the next branching instruction is stored in the first branch target address information buffer. This limitation, although not explicitly taught by Asato, is deemed inherent. Asato's Fig.6B is just one example of the embodied invention, i.e., the locations of branches within each of the sequences are clearly arbitrary and exemplary. One would realize that the first sequence of "A" instructions could include two branches, as is shown in the second sequence ("B" instructions). If the first sequence did contain two branches (like the "B" sequence), then this limitation of applicant's claim is anticipated. For instance, assume that instruction A4 was a branch. Instruction A4 would be the next branching instruction in the first sequence. In

response to encountering A4, target information of A4 would be tagged and buffered (just like it is for B4's target information).

h) when said branching instruction detection portion detects a second branching instruction in said branch target instruction sequence, a second branch target address information of the second branching instruction is stored in the second branch target address information buffer. See Fig.6B, and note that when a second branching instruction (B3) is encountered in the second sequence, its target information is tagged and buffered.

i) when said first branching instruction is executed, depending on the execution result of the first branching instruction, said branch target address information in either the first or second branch target address information buffer is invalidated and another branch target instruction sequence starts to be fetched and stored in said instruction buffer based on the branch target address information which is not invalidated. See Fig.7, and note that when a branch's outcome is known, a corresponding tag associated with that direction is broadcasted. The path's tag that does not match the broadcasted tag is invalidated. For instance, looking at Fig.6B and Fig.7, if branch A3 is taken, then tag "00 11 00 00" is broadcasted. As a result, A3's sequential path would be invalidated because it corresponds to a different tag (thereby correctly allowing execution along the target path). The buffer locations that have been invalidated (essentially hold no data), may now be allocated to new target information.

32. Referring to claim 2, Asato has taught an information processing device which reads, buffers, decodes, and executes instructions from an instruction store portion by pipeline processing, comprising:

a) an instruction reading request portion which assigns a read address to said instruction store portion. See Fig. 1, component 12, and column 5, lines 12-14.

b) an instruction buffering portion including a plurality of instruction buffers which buffer instruction sequences read from said instruction store portion. See Fig. 1, components 22A-H (reservation stations). Reservation stations buffer instructions sequences and operands. Also, note instruction cache 16. A cache is essentially a large buffer with many entries. This can also be viewed as a number of sub-buffers.

c) an instruction execution unit which decodes and executes instructions buffered by said instruction buffering portion. See Fig. 1 components 20 and 24A-H.

d) a branching instruction detection portion which detects a branching instruction inside the instruction sequences read from said instruction store portion. See lines 5-7 of the abstract and note that branches are detected by a "detection portion".

e) a branch target address information buffering portion including at least first and second branch target address information buffers which, when said branching instruction detection portion has detected a branching instruction, buffer a branch target address information for generating the branch target address of said branching instruction. See Fig. 1, components 22A-H, Fig. 6B, and column 11, lines 13-15. Note that target information is also stored in reservation stations. It should be noted from Fig. 1 that there are a plurality of reservation stations (buffers), which are table-like memories. Clearly, each individual instruction will have its own separate buffer location (entry in the table) within the reservation station. Hence, the branch target information buffers would comprise the reservation station entries dedicated to buffering the target path information.

f) wherein a first instruction sequence being processed is stored in either one of the first or second instruction buffers and when said branching instruction detection portion detects a branch instruction inside said first instruction sequence, a second instruction sequence of the branch target is stored in the other one of the first or second instruction buffers in accordance with the branch target address information of said branching instruction. See Fig.6B and column 11, lines 13-15, and note that when a branch instruction A3 in the first sequence of instructions ("A" instructions) is encountered, a target sequence ("B" instructions) are fetched, tagged, and buffered. It should be noted that the "A" instructions and the "B" instructions cannot physically be in the exact same locations within the buffer. Consequently, the locations dedicated to holding the "A" instructions make up the first buffer (e-1, for instance), whereas the locations dedicated to holding the "B" instructions make up the second buffer (e-2, for instance).

g) the branch target address information of a next branching instruction inside said first instruction sequence is stored in either one of the first or second branch target address information buffers. This limitation, although not explicitly taught by Asato, is deemed inherent. Asato's Fig.6B is just one example of the embodied invention, i.e., the locations of branches within each of the sequences are clearly arbitrary and exemplary. One would realize that the first sequence of "A" instructions could include two branches, as is shown in the second sequence ("B" instructions). If the first sequence did contain two branches (like the "B" sequence), then this limitation of applicant's claim is anticipated. For instance, assume that instruction A4 was a branch. Instruction A4 would be the next branching instruction in the first sequence. In response to encountering A4, target information of A4 would be tagged and buffered (just like it is for B4's target information).

h) the branch target address information of the branching instruction inside said second instruction sequence is stored in the other one of said first or second branch target address information buffers. See Fig.6B, and note that when a second branching instruction (B3) is encountered in the second sequence, its target information is tagged and buffered. Again, it should be realized that the first target information and the second target information cannot physically populate the exact same locations within the buffer. Consequently, the locations dedicated to holding the first target information make up the first information buffer (b-1, for instance), whereas the locations dedicated to holding the second target information make up the second information buffer (b-2, for instance)

i) wherein the first or second branch target address information buffer is selected based on the execution result of the branching instruction inside said first instruction sequence. See Fig.7, and note that when a branch's outcome is known, a corresponding tag associated with that direction is broadcasted. The path's tag that matches the broadcasted tag is validated/selected. For instance, looking at Fig.6B and Fig.7, if branch A3 is taken, then tag "00 11 00 00" is broadcasted. As a result, A3's target path would be validated because it corresponds to the same tag (thereby correctly allowing execution along the target path). The target information according to the branch in the target sequence will now be selected, as the branch corresponding to that target information is in the target sequence which was validated.

33. Referring to claim 3, Asato has taught an information processing device as described in claim 2. Furthermore, the first paragraph of claim 3 is rejected for the same reasons set forth in the rejection of claim 2(f), (g), and (h), above. In addition, Asato has taught:

a) if the execution of the branching instruction inside said first instruction sequence has resulted in branching, said first instruction sequence and the branch target address information of the next branching instruction inside said first instruction sequence are invalidated. See Fig.6B and Fig.7, and note that if branching occurs from the first sequence, then the rest of the first sequence ("A" instructions), including the next branch within the first sequence, would be invalidated because the sequential path is not desired; the target path is desired. This is done by tag broadcasting/comparing.

b) a third instruction sequence of the branch target of the branching instruction inside said second instruction sequence is stored in one of said first or second instruction buffers, in accordance with the branch target address information which have been stored in the other one of said first or second branch target address information buffers. See Fig.6B, and note that a third sequence ("C" instructions), which corresponds to the target of branch B3 in the second sequence, is tagged and buffered.

c) the branch target address information of the next branching instruction inside said second instruction sequence is stored in one of the first or second branch target address information buffers, and the branch target address information of the branching instruction inside said third instruction sequence is stored in the other one of said first or second branch target address information buffers. See Fig.6B and note that target information for branch B4 in the second sequence would be tagged and buffered, and although not explicitly taught in the example given by Asato, a branch instruction could exist in the "C" sequence, in which case, its target information would be tagged and buffered. Again, this target information (for both branches) cannot be stored in the exact same locations. So, the locations dedicated to the first target

information make up the first information buffer, whereas the locations dedicated to the second target information make up the second information buffer.

34. Referring to claim 4, Asato has taught an information processing device as described in claim 2. Furthermore, the first paragraph of claim 4 is rejected for the same reasons set forth in the rejection of claim 2(f), (g), and (h), above. In addition, Asato has taught:

a) if the execution of the branching instruction inside said first instruction sequence has not resulted in branching, said second instruction sequence and the branch target address information of the branching instruction inside said second instruction sequence are invalidated. See Fig.6B and Fig.7, and note that if branching occurs from the first sequence, then the target sequence ("B" instructions), including the branch within the second sequence, would be invalidated because the target path is not desired; the sequential path is desired. This is done by tag broadcasting/comparing.

b) a fourth instruction sequence of the branch target of the next branching instruction inside said first instruction sequence is stored in one of said first or second instruction buffers, in accordance with the branch target address information which have been stored in the other one of said first or second branch target address information buffers. See Fig.6B and note that although not explicitly taught in the example given by Asato, another branch instruction could exist in the "A" sequence after A3, in which case, its target information would be tagged and buffered. Again, this target information (for both branches) cannot be stored in the exact same locations. So, the locations dedicated to the first target information make up the first information buffer, whereas the locations dedicated to the second target information make up the second information buffer.

c) the branch target address information of the next branching instruction inside said first instruction sequence is stored in one of the first or second branch target address information buffers, and the branch target address information of the branching instruction inside said fourth instruction sequence is stored in the other one of said first or second branch target address information buffers. As discussed above, all next branch target information is tagged and buffered.

35. Referring to claim 6, the examiner has noted that claim 6 and claim 1 are nearly identical except for the fact that claim 6 includes a limitation in which a branching instruction detection portion detects branching prediction information. However, Asato has taught detecting branch predictions. See Fig, component 14, and column 13, lines 44-62. All other limitations of claim 6 are rejected for the same reasons set forth in the rejection of claim 1 above.

36. Referring to claim 7, Asato has taught an information processing device as described in claim 6. Asato has further taught that whether said branch target address information buffering portion buffers the branch target address information of said branching instruction is determined in accordance with the branching prediction information of the branching instruction which is detected by said instruction detection portion. See column 13, lines 55-62.

37. Referring to claim 8, Asato has taught an information processing device as described in claim 6. Asato has further taught that whether said instruction buffering portion fetches the branch target instruction sequence of said branching instruction is determined in accordance with the branching prediction information of the branching instruction which is detected by said instruction detection portion. See column 13, lines 55-62.

38. Referring to claim 9, Asato has taught an information processing device as described in claim 6. Asato has further taught if said branching instruction detection portion predicts with a prescribed high level of probability that the branching instruction will not branch, said branch target address information buffering portion does not fetch the branch target instruction sequence of said branching instruction. See column 13, lines 55-62, and note that if a branch is predicted not-taken, the sequential path is fetched, not the target side.

39. Referring to claim 12, Asato has taught an information processing device with pipeline processing comprising:

a) an instruction fetch portion which fetches both a sequential side instruction sequence and a target side instruction sequence of a branch instruction. See the abstract, Fig.1, and Fig.6B, and note that both a target and sequential side are fetched and tagged. In addition this fetching and tagging occurs despite branch prediction. See column 13, lines 44-62.

b) a cache controller which fetches instructions from a cache memory or from a main memory in response to a fetch request from said instruction fetch portion. See Fig.1, component 12.

c) a memory bus access portion which accesses said main memory. See Fig.1, component 12, and column 5, lines 12-14.

d) an instruction buffer which buffers instructions which have been fetched. See Fig.1, components 22A-H (reservation stations). Reservation stations buffer instructions sequences and operands. Also, note instruction cache 16. A cache is essentially a large buffer with many entries. This can also be viewed as a number of sub-buffers.

e) a branching prediction portion which, prior to an execution of a branching instruction, performs a branching prediction for the branching instruction which is stored in said instruction buffer. See Fig.1, component 14.

f) if the branching direction of said branching instruction is not yet determined, said cache controller performs a memory bus access to said main memory according to a branching direction predicted by the branching prediction portion. See column 13, lines 55-62, and note that when a branch prediction occurs (in this case, assume the branch is predicted not-taken), a block of instructions would be fetched along the sequential path. The fetch address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there is a cache miss, slower levels of memory, including main memory, would be accessed in order to retrieve the desired instructions, as is known in the art. This is the inherent nature of a memory hierarchy.

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asato, as applied above.

42. Referring to claim 5, Asato has taught an information processing device as described in claim 1. Asato has not explicitly taught that in response to a single instruction read request from

said instruction reading request portion, a plurality of consecutive instructions from said read address are read from said instruction store portion (main memory) and buffered in said instruction buffering portion. However, Asato has taught reading blocks of instructions at a time during a single fetch. See column 5, lines 33-35. A person of ordinary skill in the art would have recognized that the more instructions that can be fetched at a time, the less amount of times the system would to make a expensive access to main memory. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Asato such that Asato's main memory is also fetched from in blocks (i.e., plurality of instructions at once).

43. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asato, as applied above, in view of Hara, U.S. Patent No. 5,740,415 (as applied in the previous Office Action)

44. Referring to claim 10, Asato has taught an information processing device as described in claim 6. Asato has not taught that when said branch target address information buffering portion has buffered branch target address information of a first branching instruction, if said branching instruction detection portion has detected a second branching instruction which has a greater possibility of branching than said first branching instruction, said branch target address information buffering portion invalidates the branch target address information of said first branching instruction and buffers the branch target address information of said second branching instruction. However, Hara has taught such a concept. See column 9, lines 4-10. As disclosed by Hara, by storing a branch instruction having a high branch probability as opposed to an instruction with a small branch probability, branch prediction accuracy is improved. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to

modify Asato's branch target address information buffer so that it operates in a manner equal to that of Hara's.

45. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asato, as applied above, in view of Shiell, U.S. Patent No. 5,864,697 (as applied in the previous Office Action).

46. Referring to claim 11, Asato has taught an information processing device as described in claim 6. Asato has not taught, but Shiell has taught, that when the instruction buffer of said instruction buffering portion is empty (it should be noted that whether the instruction buffer is empty or not, the following still hold true):

a) if a first branching instruction having a first branching possibility is detected by said branching instruction detection portion, a branch target instruction sequence of said first branching instruction is not fetched to said instruction buffering portion and said branch target address information buffering portion buffers the branch target address information of the first branching instruction. If the first branch instruction has a very low branching possibility and it is predicted not-taken by the BTB, then the target instruction sequence for that branch will not be fetched and buffered. Instead, the next sequential instruction is fetched. See column 2, lines 11-31 (specifically, lines 18-21). Regardless, the branch target address information buffering portion (BTB) will buffer the branch target address information such that the target address will be buffered along with the history update based on the outcome of the branch. See column 2, lines 15-22.

b) if said branching instruction detection portion has detected a second branching instruction which has a second branching possibility which is higher than said first branching possibility, a

branch target instruction sequence of said second branching instruction is fetched to said instruction buffering portion. If the second branch instruction has a very high branching possibility and it is predicted taken by the BTB, then the target instruction sequence for that branch will be fetched and buffered. See column 2, lines 11-31 (specifically, lines 18-21). According to Shiell's abstract, such function is part of a system which allows for more accurate predictions, by tracking more history, while keeping the storage requirement for the predictor low. Consequently, in order to increase prediction accuracy while limiting the amount of hardware, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Asato to include the concept of Shiell.

47. Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asato in view of Lee et al., Instruction Cache Fetch Policies for Speculative Execution, 1995 (as applied in the previous Office Action and herein referred to as Lee).

48. Referring to claim 13, Asato has taught an information processing device as described in claim 12.

a) while the branching direction of said branching instruction is not yet determined, if the cache controller has performed a cache miss with respect to an instruction in the predicted branching direction of said branching instruction, said cache controller performs the memory bus access to the main memory for an instruction fetch. See column 13, lines 55-62, and note that when a branch prediction occurs (in this case, assume the branch is predicted not-taken), a block of instructions would be fetched along the sequential path. The fetch address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there

is a cache miss, slower levels of memory, including main memory, would be accessed in order to retrieve the desired instructions, as is known in the art. This is the inherent nature of a memory hierarchy.

b) Asato has not taught that while the branching direction of said branching instruction is not yet determined, if said cache controller has performed a cache miss with respect to an instruction which is not in the predicted branching direction, said cache controller does not perform the memory bus access and stops said instruction fetch. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Asato such that if said cache controller has performed a cache miss with respect to an instruction which is not in the predicted branching direction, said cache controller does not perform the memory bus access and stops the instruction fetch.

49. Referring to claim 14, Asato has taught an information processing device as described in claim 12.

a) Asato has not taught that while the branching direction of said branching instruction is not yet determined and the predicted branching direction of said branching instruction is the sequential side, in the event of said cache controller performing a cache miss with respect to said target side instruction, said cache controller does not perform a memory bus access and stops said

instruction fetch. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Asato such that if said cache controller has performed a cache miss with respect to said target side instruction, said cache controller does not perform a memory bus access and stops the instruction fetch.

50. Referring to claim 15, Asato has taught an information processing device as described in claim 12. Asato has not taught that while the branching direction of said branching instruction is not yet determined, said cache controller does not perform a memory bus access after a cache miss depending on the predicted branching direction of said branching instruction. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Asato such that the cache controller does not perform a memory bus access after a cache miss depending on the predicted branching direction of said branching instruction.

51. Referring to claim 16, Asato has taught an information processing device with pipeline processing, comprising:

a) an instruction fetch portion which fetches both a sequential side instruction sequence and a target side instruction sequence of a branching instruction in spite of a branching prediction of the branching instruction. See the abstract, Fig.1, and Fig.6B, and note that both a target and sequential side are fetched and tagged. In addition this fetching and tagging occurs despite branch prediction. See column 13, lines 44-62.

b) a cache controller which fetches instructions from a cache memory or from a main memory in response to a fetch request from said instruction fetch portion. See Fig.1, component 12.

c) a memory bus access portion which accesses said main memory. See Fig.1, component 12, and column 5, lines 12-14.

d) an instruction buffer which buffers instructions which have been fetched. See Fig.1, components 22A-H (reservation stations). Reservation stations buffer instructions sequences and operands. Also, note instruction cache 16. A cache is essentially a large buffer with many entries.

e) a branching prediction portion which, prior to an execution of a branching instruction, performs a branching prediction of the branching instruction which is stored in said instruction buffer. See Fig.1, component 14.

f) if a branching direction of said branching instruction has been determined and said cache controller performs a cache miss with respect to an instruction in the determined branching direction, said cache controller performs a memory bus access. See column 5, lines 52-54, column 7, lines 38-44, and column 7, lines 11-18. Note that when a branch prediction occurs (in

this case, assume the branch is predicted taken), the target address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there is a cache miss, slower levels of memory, including main memory, may have to be accessed in order to retrieve the desired instructions, as is known in the art. This is the inherent nature of a memory hierarchy.

g) Asato has not taught that if the branching direction of said branching instruction is not yet determined and said cache controller performs a cache miss with respect to an instruction fetch, said cache controller does not perform a memory bus access and stops said instruction fetch. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Asato such that if the branching direction of said branching instruction is not yet determined and said cache controller performs a cache miss with respect to an instruction fetch, said cache controller does not perform a memory bus access and stops the instruction fetch.

h) if said branching direction of said branching instruction has been determined and said cache controller performs a cache miss with respect to an instruction in the determined branching direction, said cache controller performs a memory bus access. See column 5, lines 52-54, column 7, lines 38-44, and column 7, lines 11-18. Note that when a branch prediction occurs (in

this case, assume the branch is predicted taken), the target address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there is a cache miss, slower levels of memory, including main memory, may have to be accessed in order to retrieve the desired instructions, as is known in the art. This is the inherent nature of a memory hierarchy.

52. Referring to claim 17, Asato in view of Lee has taught an information processing device as described in claim 16. Asato has further taught that if the branching direction of said branching instruction is not yet determined, an instruction for which a cache hit has been made is prefetched and stored in said instruction buffer. It should be realized that before a branch's direction is determined, instructions along the predicted path will be fetched from memory. If a cache hit occurs, these instructions are brought in from the cache and placed into the instruction buffer (reservation station). See column 13, lines 44-62.

53. Referring to claim 18, Asato in view of Lee has taught an information processing device as described in claim 16. Asato has further taught that instructions are selected from either said instruction sequential side or instruction target side in said instruction buffer depending on the branching direction of the branching prediction portion, and decoded. See column 13, lines 55-62, and note that a not-taken prediction results in fetching of sequential-side instructions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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DJH
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August 10, 2005

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